# caeleste

#### Hybrid photon counting and ranging APD array

sens

B. Dierickx<sub>1,3</sub>, S. Bellis<sub>2</sub>, N.Witvrouwen<sub>1</sub>, <u>B. Dupont<sub>1,4</sub></u>, C. Jackson<sub>2</sub>

Caeleste, Antwerp, Belgium
 sensL, Cork, Ireland
 Vrije Universiteit Brussel, Belgium

4 Université Paris Nord XIII, France

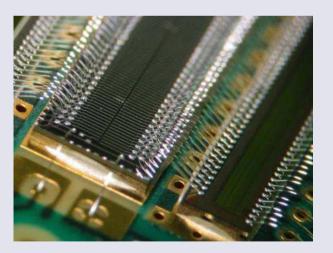


Presented at CNES CMOS detector Workshop, Toulouse, Dec 2009

### Challenge addressed

 In this paper we present the concept, design and results of a hybrid combination of:

- a 128 linear APD detector array
- and 2 Silicon ROIC
- realizing



 $\rightarrow$ 15 bit photon counting mode

→15 bit distance ranging, by counting, with clock period resolution (100MHz)  $\rightarrow$ increased accuracy distance ranging accuracy by analog interpolation, to 150ps (2cm)

#### outline



- SPAD background
- Brief specifications
- Pixel features
- ROIC and detector design
- Performance & Measurements
- Conclusions and perspectives

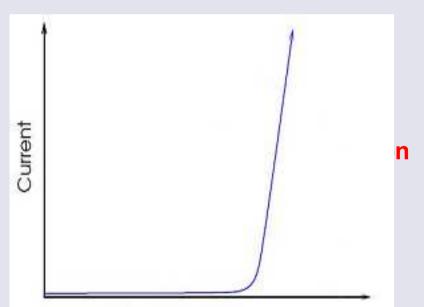
#### outline



- SPAD background
- Brief specifations
- Pixel features
- ROIC and detector design
- Performance & Measurements
- Conclusions and perspectives



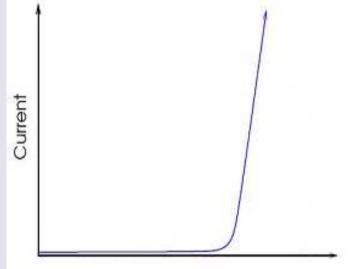
- SPADS or "Geiger-Mode" APD
  - APD designed to operate beyond breakdown voltage



- In this case
  - it is a silicon detector for visible light
  - breakdown voltage is about 28 V



- SPAD operation:
  - RESET:
  - APD is brought to higher than breakdown bias voltage

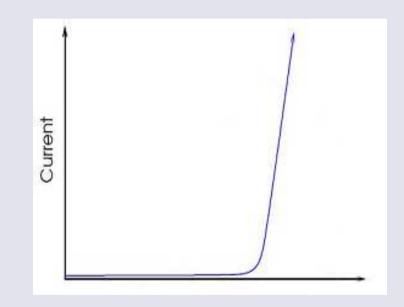


- Electric field is high
- initial electron is required to initiate the avalanche breakdown

# caeleste sensl

#### SPAD operation: Sensing

 An electron is generated in the depletion region due to photoelectric effect (or dark current)



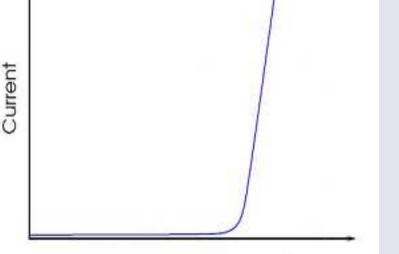
- The avalanche starts, the APD is going into breakdown

14 December 2009

# caeleste sens

#### • SPAD operation: Sensing (2)

- Current increases dramatically
- The bias voltage drops rapidly due to resistive load of external circuit

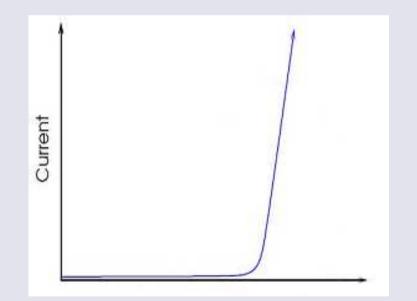


 That voltage drop is sensed by the ROIC sense amplifier

14 December 2009



- SPAD operation: Active Quenching
  - After breakdown one must "quench" the diode

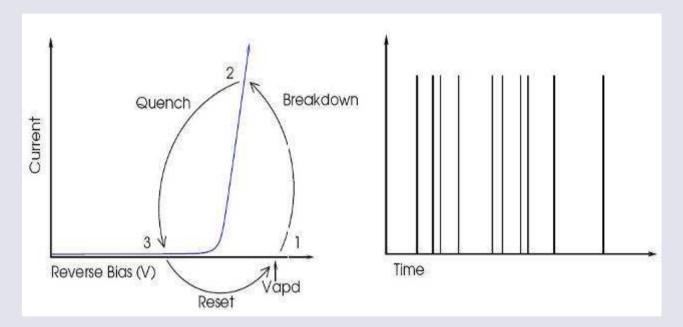


 The quenching operation makes sure that no residual free charge is present, thus allows the next reset to happen

14 December 2009

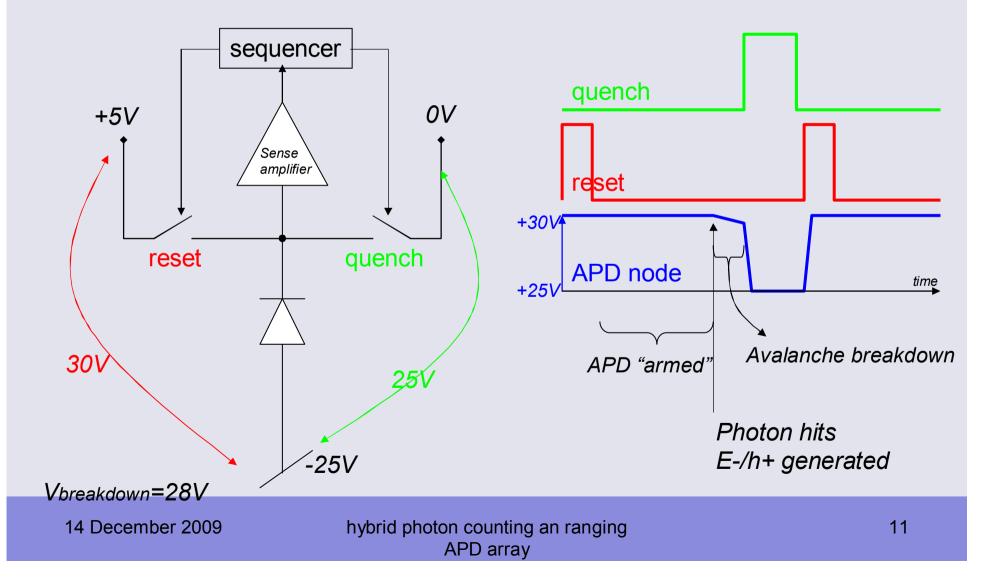
# caeleste sens

#### Summary



## caeleste sensL

#### active quench/reset



#### outline



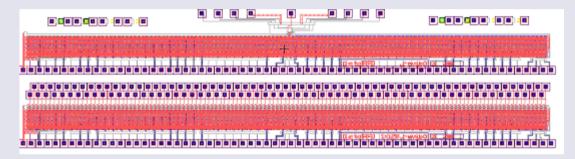
- SPAD background
- Brief specifations
- Pixel features
- ROIC and detector design
- Performance & Measurements
- Conclusions and perspectives

#### **Specifications**

# caeleste sensl

#### Scalable ROIC design

- Pixel pitch: 100um
- 479T per pixel
- 15bits counter in-pixel



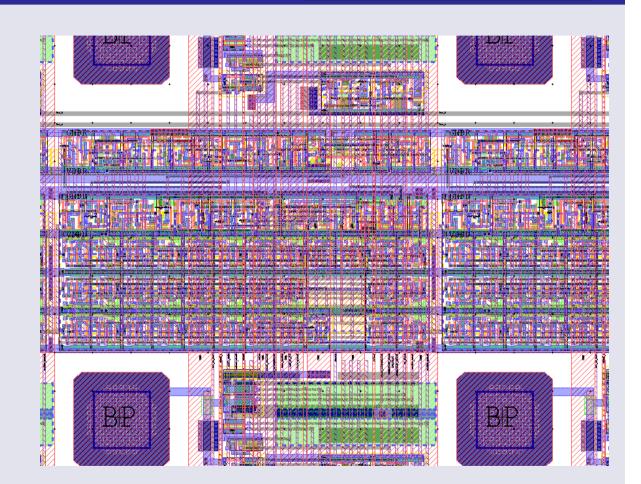
- Geiger mode, up to 20MHz count frequency, (APD limited)
- Ranging mode, 100MHz timer/counter
- Ranging time accuracy: 150ps
- Analog interpolation for ranging
- Power dissipation 100~150 mW on 128x1 device, depending on mode

#### outline



- SPAD background
- Brief specifations
- Pixel features
- ROIC and detector design
- Performance & Measurements
- Conclusions and perspectives

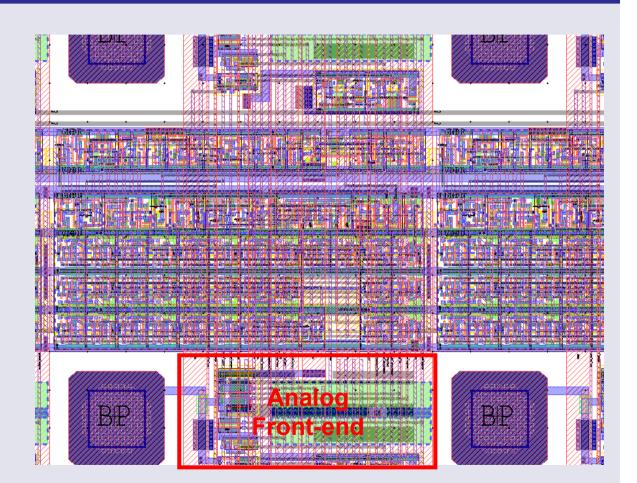
- Mixed mode pixel
- 100x100um
- 479 MOSFETs



eles

sens

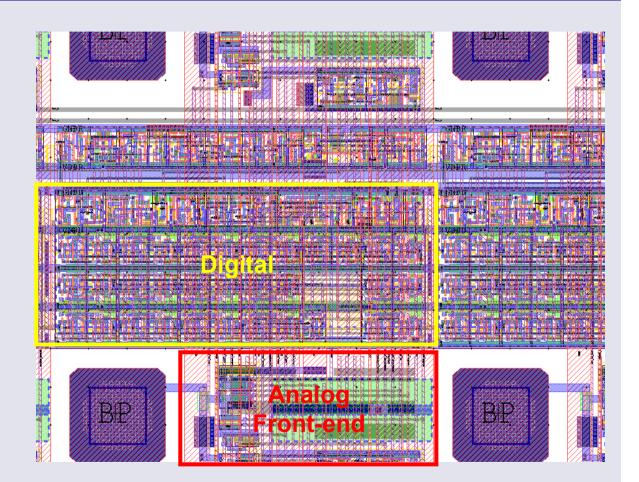
- Mixed mode pixel
- 100x100um
- 479 MOSFETs



e es

sens

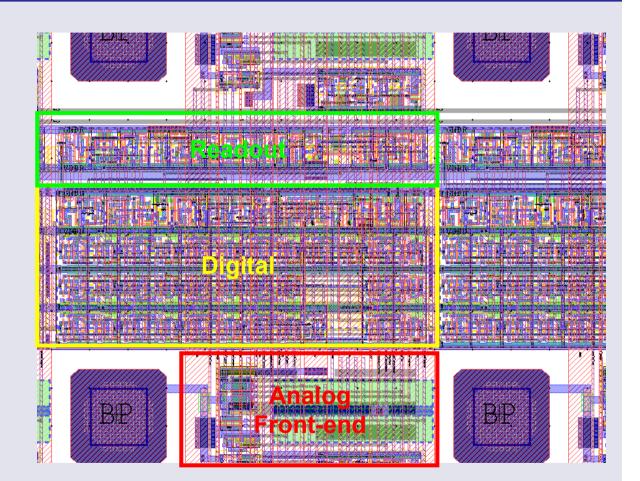
- Mixed mode pixel
- 100x100um
- 479 MOSFETs



caeles

sens

- Mixed mode pixel
- 100x100um
- 479 MOSFETs

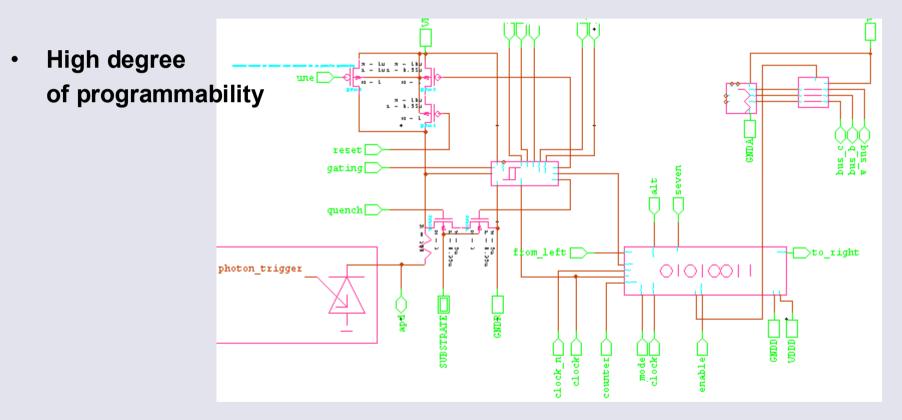


caeles

sens

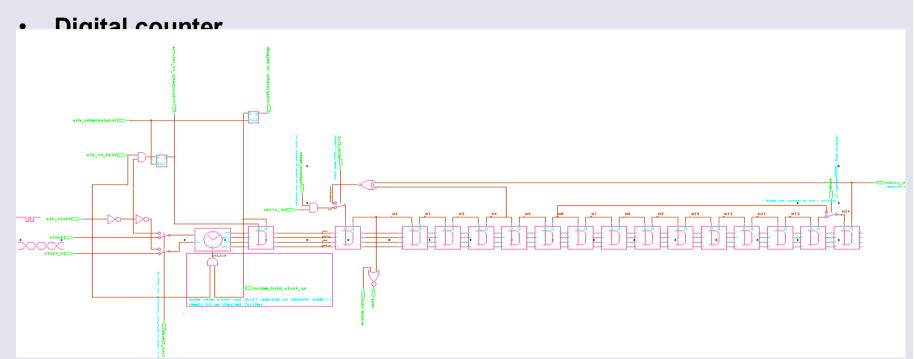


• Pixel schematic



14 December 2009





- Low power consumption, High count rate
- Designed for long Time of Flight, max 5.000m distance
- 100MHz counter = 10 ns TOF accuracy
- higher accuracy by analog interpolation between counts



#### • Digital counter Pseudo Random Code, verification example

	100MHz Acquisition / 80MHz Readout		
Gate Length (clocks)	Pseudo Random (Hex)	Pseudo Random Binary	Decoded (Hex)
5	001E	00000000011110	0005
6	003C	00000000111100	0006
7	0078	00000001111000	0007
8	00F0	00000011110000	0008
9	01E1	000000111100001	0009
10	03C3	000001111000011	<b>000A</b>
11	0787	000011110000111	000B
12	0F0F	000111100001111	000C
13	1E1E	001111000011110	000D
14	3C3C	011110000111100	000E
15	7878	111100001111000	000F
16	70F1	111000011110001	0010
17	61E2	110000111100010	0011
18	43C4	100001111000100	0012
19	0788	000011110001000	0013

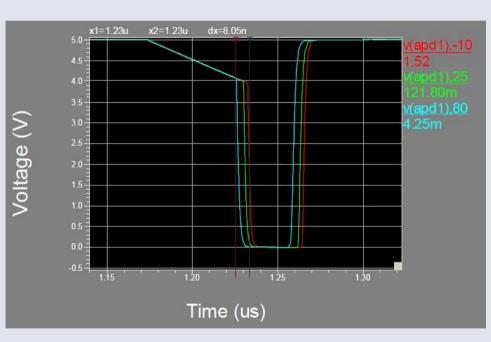
14 December 2009

### Pixel design, ranging

- However... Digital counter only is insufficient for ranging
- 100MHz count rate means 10ns discretization thus a 1.5m accuracy
- For better accuracy, an analog interpolator is used.
- As the APD fires, an analog voltage is interpolated between two clocks in the pixel memory element.

## Pixel design, ranging

- The goal is to achieve 140ps time resolution
- Is this realistic with respect to temperature?
- Simulation of the APD firing with quenching
- Circuit sensitivity is 90ps /K



→ Temperature stabilisation or calibration is mandatory

## Pixel design, Geiger

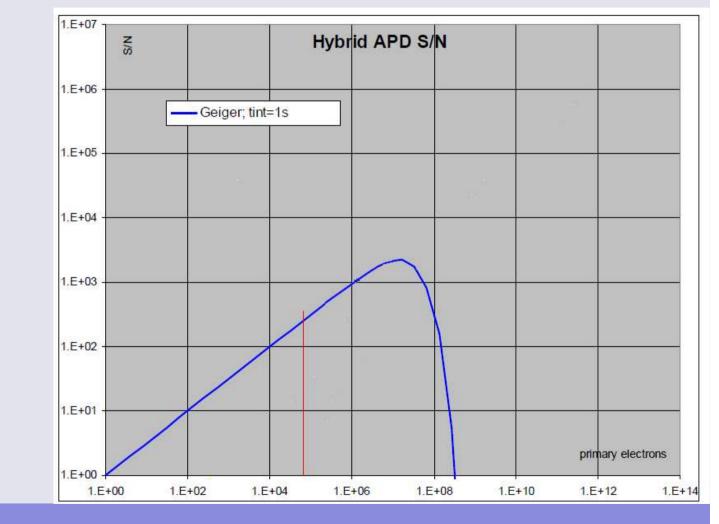
- The sensor is able to do imaging in Geiger counter mode
- In Geiger mode, each pixel counts the incoming primary electron.
- Ideally:
  - 1 primary photon = 1 primary electron
  - In counting device, the noise is limited by photon shot noise.

## Pixel design, Geiger

- The sensor is able to do imaging in Geiger counter mode
- In Geiger mode, each pixel counts the incoming primary electron.
- Ideally:
  - 1 primary photon = 1 primary electron
  - In counting device, the noise is limited by photon shot noise.
- However:
  - The pixel operation (reset, sense, quench.) requires time: 50ns
  - Thus, with a given exposure time, the S/N will roll off at high flux

## Pixel design, Geiger

# caeleste sensL



14 December 2009

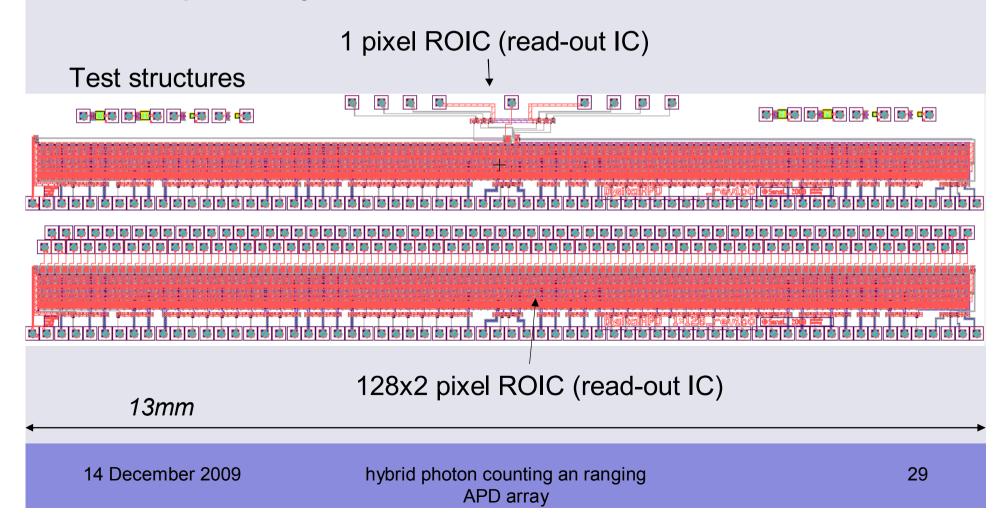
#### outline



- SPAD background
- Brief specifations
- Pixel features
- ROIC and detector design
- Performance & Measurements
- Conclusions and perspectives

### **ROIC** design

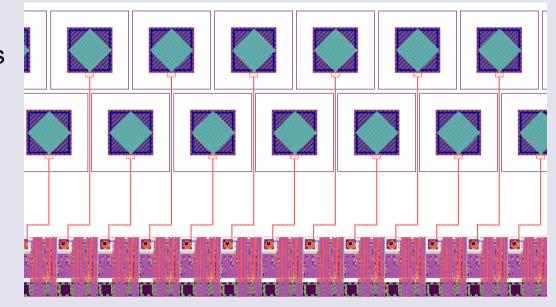
• The pixel array is scalable.



sei

### **ROIC** design

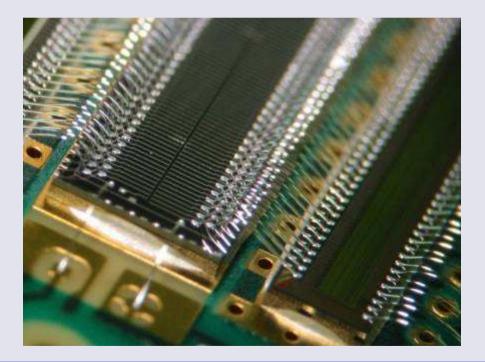
- The pixel array is scalable
- It is designed for lateral wire bonding
  - One row of 128 pixels
  - Two rows of 128 pixels interleaved



ser

### **ROIC** design

- The pixel array is scalable
- It is designed primarily for lateral wire bonding
  - One row of 128 pixels
  - Two rows of 128 pixels interleaved
  - 256 bondpads to APDs
  - 136 bondpads to board



**PPS** 

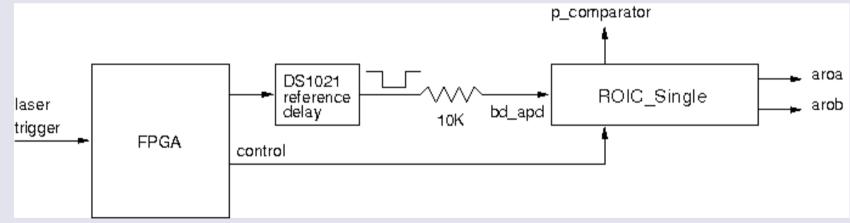
sens

### **ROIC** interfacing

# caeleste sensL

#### DIGITAL

- differential LVDS output, up to 100MHz
- Compatible with DS1021 reference timing generator
- Accurately controls the timing of the triggering of the quench circuit



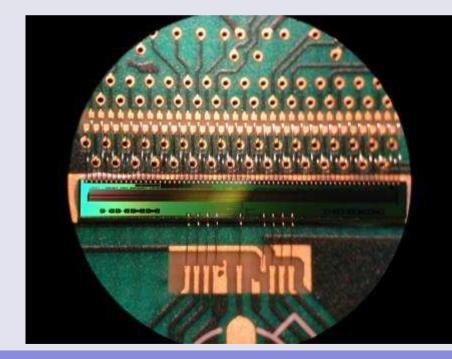
#### ANALOG

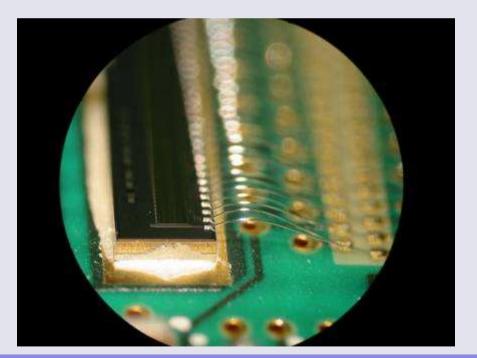
- Pseudo Differential analog output
- 15MHz pixel readout rate

#### Hybrid assembly



- Single detector version
- 73 wirebonds, chip on board



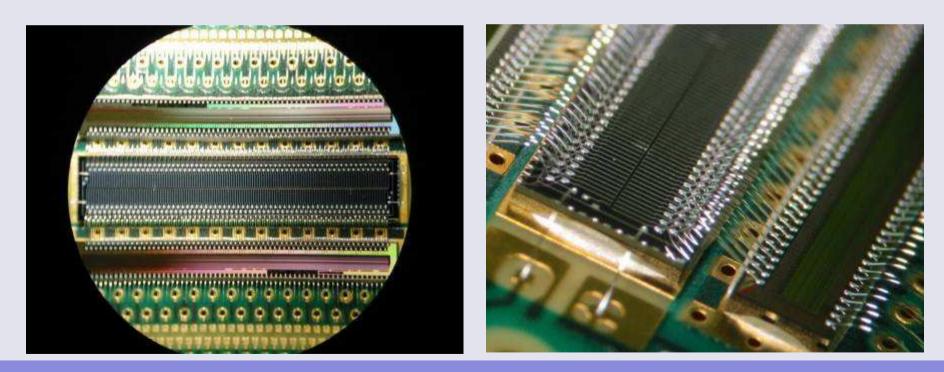


14 December 2009

#### Hybrid assembly



- 2x128 ROIC
- 256 APD detector array



14 December 2009

#### outline

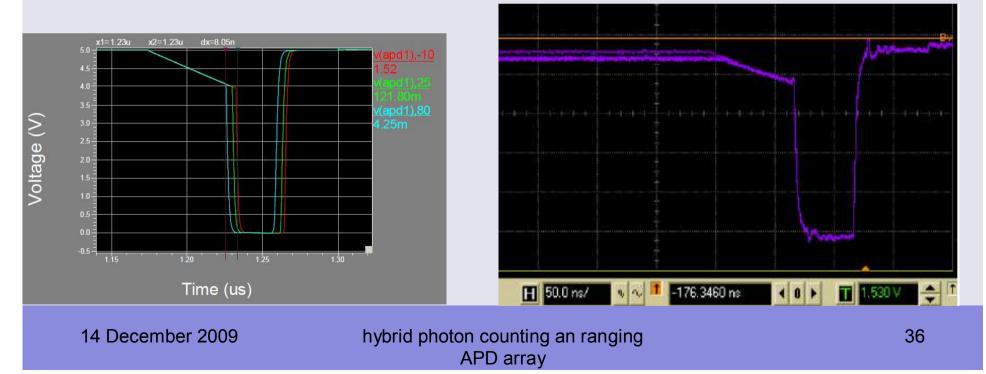


- SPAD background
- Brief specifations
- Pixel features
- ROIC and detector design
- Performance & Measurements
- Conclusions and perspectives

#### Performance

# caeleste sens

- Several chips have been assembled
  - Single row or dual rows
  - Tested with resistive load first, then discrete photodiodes and APD arrays



#### Performance

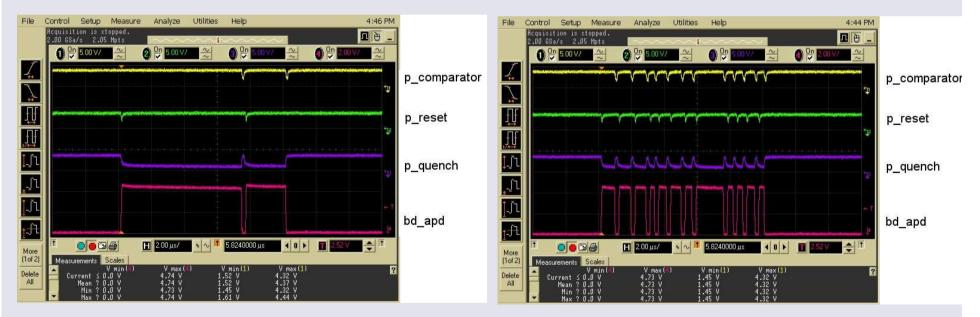


• Quench, Sense circuit and Reset timing:

#### Response of a 50µm APD

**Dark condition** 

illuminated condition

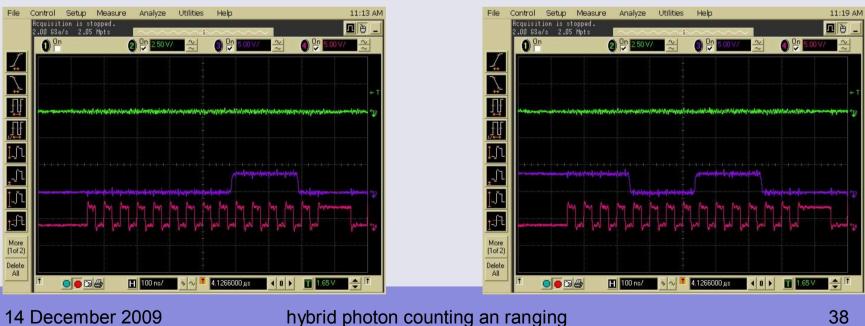


14 December 2009

caeleste sensL

- Digital testing:
  - Acquisition : 10...100 MHz
  - Readout: 10...80 MHz
    Gate duration 2 clocks
    PRC: 003C Decoded:0006

#### Gate duration 11 clocks PRC: 7878 Decoded:000F



APD array



- Time of flight testing
- Experiment:
  - ROIC is electrically triggered
  - Trigger is swept with 100ps step over 25ns
  - DIGITAL count is recorded
  - ANALOG interpolated value is recorded

# caeleste sensL

#### ROIC TAC circuit testing @50ns delay



14 December 2009

# caeleste sensL

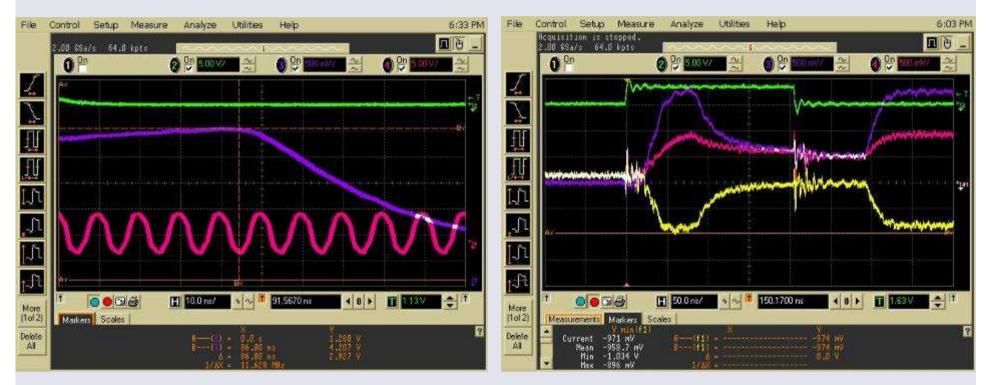
#### ROIC TAC circuit testing @51ns delay



14 December 2009

# caeleste sensL

#### ROIC TAC circuit testing @52ns delay



14 December 2009

# caeleste sensL

#### ROIC TAC circuit testing @53ns delay



14 December 2009

# caeleste sensL

#### ROIC TAC circuit testing @54ns delay



14 December 2009

# caeleste sensL

#### ROIC TAC circuit testing @55ns delay



14 December 2009

# caeleste sensL

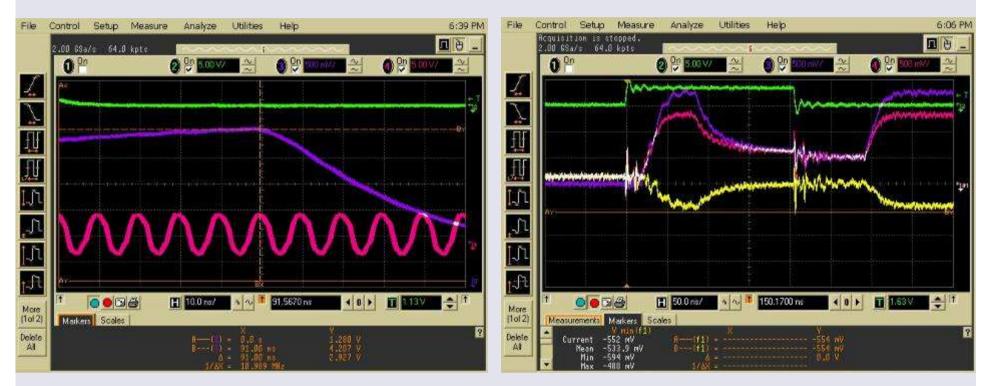
#### ROIC TAC circuit testing @56ns delay



14 December 2009

# caeleste sensL

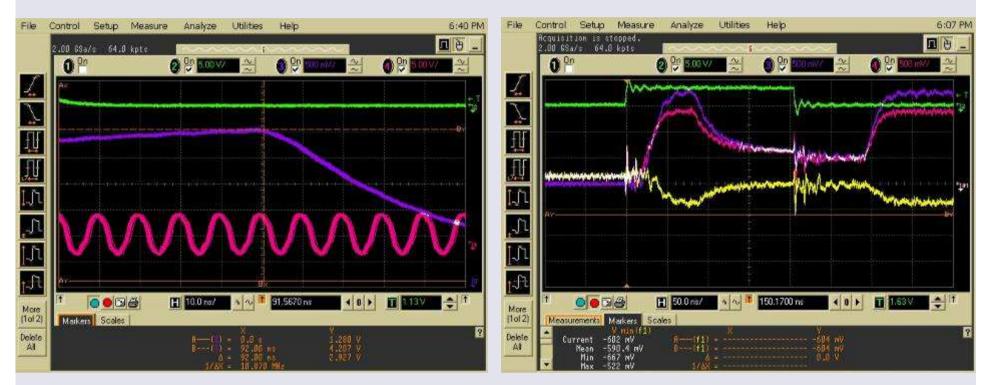
#### ROIC TAC circuit testing @57ns delay



14 December 2009

# caeleste sensL

#### ROIC TAC circuit testing @58ns delay



14 December 2009

# caeleste sensL

#### ROIC TAC circuit testing @59ns delay



14 December 2009

# caeleste sensL

#### ROIC TAC circuit testing @60ns delay



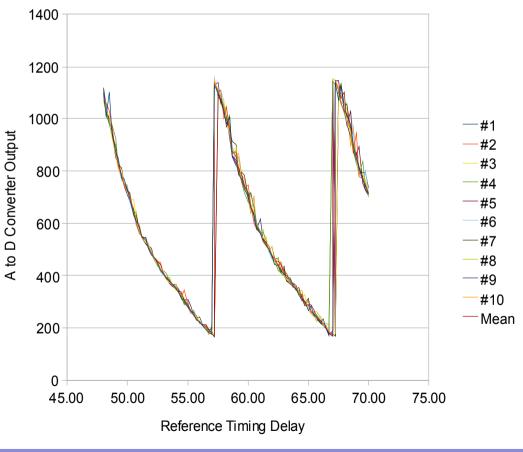
14 December 2009

# caeleste sensL

#### Digitally converted interpolated output

- Standard deviation
  measured 14 LSB<sub>RMS</sub>
  average
- Corresponds to accuracy of 14 x 11ps/lsb = 154ps<sub>RMS</sub>

→2cm distance resolutionOver 5000 m dynamic



14 December 2009

### outline



- SPAD background
- Brief specifations
- Pixel features
- ROIC and detector design
- Performance & Measurements
- Conclusions and perspectives

### conclusions



#### Conclusion

- Sophisticated APD+ROIC pixel with multiple modes of operation
  - Geiger mode (SPAD) counting
  - Distance ranging, digital at 100MHz
  - Analog interpolation of distange ranging
  - 15bit and 7bit counting
- Hybridization of ADP array and ROIC
- System built around APD and ROIC
- We demonstrated a 2cm accuracy ranging with 5.000m dynamic

### conclusions



#### Perspective

- APD will continue to be tested in *imaging* Geiger mode as well
- The pixel design is also foreseen to be instantiated in a 2D array, to be studied





 Caeleste and sensL would like to acknowledge their partners:

ESA (WP7 framework)





